Please amend the paragraph beginning on page 5, line 14, as follows:

Referring to Figure 5, a cross-section of an alternate embodiment capacitor 300 is illustrated. While the embodiment of Figure 2 included strips of conductors that formed a pyramid-shaped cross-section, the present embodiment can be fabricated with full layers of conductors. The capacitor 300 includes a substrate 302. A first layer of conductor 304 is located over the substrate. An second conductive layer 308 is separated from the first conductor by dielectric layer 306. Likewise dielectric layers 310 and 314 surround a [top conductor] third conductive layer 312. First electrical vias 316 are used to connect the first and third [conductors] conductive layers 304, 312. A clearance is provided in layer 308 to isolate the first electrical vias 316 from the second [conductor layer] conductive layer 308. Second electrical vias 318 contact the second conductive layer 308. Clearance areas are provided in the first [conductor] conductive layer 304 to isolate the second electrical vias 318 from the first [conductor layer] conductive layer 304. C4 lands 320 can be provided to allow the capacitor 300 to be mounted to a circuit board. In this embodiment the [conductor] conductive layers do not decrease in surface area as the number of layers increase.

Please amend the paragraph beginning on page 6, line 1, as follows:

In another embodiment illustrated in Figure 6, the [conductor] conductive layers are fabricated as described with reference to Figure 2. In this embodiment, however, the interconnect vias pass through the second [conductor] conductive layer to connect [both the top and bottom] the first and third conductive layers using common vias. Again, a clearance area needs to be provided in the intermediate conductor to avoid shorts between the alternate conductor layers.

Please amend the paragraph beginning on page 6, line 12, as follows:

Figure 7 illustrates a cross section of an embedded capacitor embodiment comprising a capacitor 400 that is physically coupled to a dielectric layer 402. In one embodiment, the capacitor is attached to the dielectric using an adhesive. Vias 404 are then formed through the dielectric layer to expose electrical connections on the capacitor. The vias are then plated with a conductor to [for] form an electrical interconnect to the capacitor. This embodiment, therefore, provides an alternate manner of coupling the capacitor to a circuit. Figure 8 illustrates another embodiment of the present invention where electrical vias 410 are formed through the substrate 402 of the capacitor 400. The capacitor can be fabricated as explained herein, but with the additional electrical vias 410. These vias 410 allow circuits to be coupled to both sides of the capacitor and provided a more direct conductive path between the circuits.

Please amend the paragraph beginning on page 6, line 23, as follows:

Figure 9 illustrates an embedded capacitor package 500. The capacitor 480 includes interconnect lands on each side of the capacitor and can be fabricated as illustrated in Figure 8. The capacitor has a first circuit package 450 formed on the top of the capacitor and a second